## REMARKS

In response to the Office Action mailed on April 24, 2006, Applicant respectfully requests reconsideration. Claims 1-21 were previously pending in this application. By this amendment, claims 1, 3, 15 and 14 are amended. Claims 2 and 16 are canceled. Claims 22 and 23 are added. As a result, claims 1, 3-15 and 17-23 are pending for examination with claims 1 and 14 being independent. No new matter has been added.

### I. Specification

The Office Action objects to the title as not being descriptive. Applicant respectfully disagrees. The title "DIGITAL SIGNAL PROCESSOR HAVING DATA ADDRESS GENERATOR WITH SPECULATIVE REGISTER FILE" precisely and distinctly describes the invention. Applicant is open to amending the title to overcome the rejection if the Examiner has suggestions for amendment. However, Applicant is unsure of what the Examiner feels is not descriptive about the title as, in Applicant's opinion, the title is descriptive and indicative of the invention.

### II. Overview of Embodiments of the Invention

One embodiment described in the application is directed to a method and apparatus for conserving power during the operation of a digital signal processor having a pipeline architecture. In conventional pipeline architectures, speculative data addresses generated as instructions advance through the pipeline are stored in a speculative register file. Once the speculative data address becomes architectural, the architectural data address is written to an architectural register file. Applicant has appreciated that significant power is consumed during operation as a result of reading/writing architectural data addresses between multiple register structures, which may occur on every clock cycle (*see e.g.*, Page 2, final paragraph of the specification).

According to one embodiment of the present invention, power is conserved by allocating locations in the speculative register file for one or more architectural addresses (i.e., speculative data addresses that have become architectural). Thus, as the speculative data addresses become

architectural, there may be no need to read the architectural data addresses from the speculative register file and write them to an architectural register file, thus conserving power (*see e.g.*, Page 14, first full paragraph).

The foregoing summary of one embodiment of one aspect of the invention is provided solely for the convenience of the Examiner. It should be appreciated that each of the independent claims may not be limited in the manner described in the summary above. Therefore, the Examiner is requested not to rely upon the summary for determining whether each of the claims distinguishes over the prior art of record, but to do so based solely on the language of the claims themselves and the arguments presented below.

## III. Rejections Under 35 U.S.C. §103

The Office Action rejects claims 1-5, 7, 10, 12-18 and 21 under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,960,467 (Mahalingaiah) in view of U.S. Patent No. 6,263,354 (Gandhi). Applicant respectfully traverses the rejection. While Applicant believes that the claims as previously presented distinguish over the combination of Mahalingaiah and Gandhi, Applicant has amended independent claims 1 and 14 to further the prosecution of this application. In particular, Applicant has amended the claims to clearly point out that the speculative register file is configured to store, in addition to a speculative addresses, at least one architectural address. The combination of Mahalingaiah and Gandhi is completely silent in this respect.

Mahalingaiah discloses a conventional speculative register for storing register values for instructions that have been decoded, but have not yet been executed. Mahalingaiah discloses in column 3, lines 49-53 that a "speculative register file stores speculative register values corresponding to previously decoded instructions. The speculative register values are generated prior to execution of the previously decoded instructions." Similarly, in column 7, lines 7-9, Mahalingaiah states that "[s]peculative register file 35 is provided for generating and storing registers values prior to execution of the instructions which generate those values." Mahalingaiah nowhere discloses or suggests that the speculative register file stores anything but register values relating to instructions that have yet to be executed, that is, register values that are speculative.

The only disclosure in Mahalingaiah related to the size of the speculative register file appears in column 18, line 65 – column 19, line 5, which states that "the number of storage locations within register storage 80 is equal in number to the number of lines within reorder buffer 32," which is related to the number of instructions being concurrently decoded (see FIG. 4, 4A and 4B and the corresponding description in columns 18-22). Mahalingaiah describes a speculative register file to store speculative register values, but nowhere mentions anything about the speculative register file storing one more architectural addresses. Gandhi makes no reference to speculative register files and does not cure the deficiencies of Mahalingaiah.

Claim 1, as amended, recites a digital signal processor comprising an address generator configured to generate speculative data addresses in response to an address operand and one or more address parameters, a pipelined execution unit configured to execute instructions in an instruction pipeline having a plurality of stages using data at locations specified by the speculative data addresses, a speculative register file capable of simultaneously storing at least a speculative data address for each of the plurality of pipeline stages and at least one architectural data address, the speculative register file configured to hold the speculative data addresses as corresponding instructions advance through the instruction pipeline and at least one speculative data address after the at least one speculative data address becomes a respective architectural data address, control logic configured to write speculative data addresses to the speculative register file as the speculative data addresses are generated by the address generator and to supply speculative data addresses and architectural data addresses to the address generator.

Nowhere does the combination of Mahalingaiah and Gandhi disclose or suggest a "speculative register file capable of simultaneously storing at least a speculative data address for each of the plurality of pipeline stages and at least one architectural data address," as recited in claim 1. Therefore, claim 1 patentably distinguishes over the combination of Mahalingaiah and Gandhi and is in allowable condition.

Claims 3-13 and 22 depend from claim 1 and are allowable for at least the same reasons.

Claim 14, as amended, recites a method for operating a digital signal processor, the method comprising generating a speculative data address in response to an address operand and one or more address parameters, executing an instruction using data at a location specified by the speculative

data address in a pipelined execution unit, holding the speculative data address in a speculative register file as a corresponding instruction advances through the pipeline, holding one or more speculative data addresses that have become architectural data addresses in the speculative register file, and writing the speculative data address to the speculative register file as the speculative data address is generated by the address generator.

Nowhere does the combination of Mahalingaiah and Gandhi disclose or suggest "holding one or more speculative data addresses that have become architectural data addresses in the speculative register file," as recited in claim 14. Therefore, claim 14 patentably distinguishes over the combination and is in allowable condition.

Claims 15, 17-21 and 23 depend from claim 14 and are allowable for at least the same reasons.

## CONCLUSION

In view of the above remarks, Applicant believes the pending application is in condition for allowance, and a Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
***James F. Galeotos et al., Applicant***

By: William R. McClellan

William R. McClellan, Reg. No. 29,409
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Telephone: (617) 720-3500

Docket No. A0312.70525US00
Date: September 25, 2006
**x09/24/06x**